In response to the statement that the original specification does not disclose interconnected transistors in and at the surface of the device silicon layer, as claimed in claims 1, 7, and 10, the Examiner's attention is respectfully directed to FIG. 3g and its description at page 7, lines 5-7, of the instant specification: "FIG. 3g schematically shows in expanded cross-sectional elevation view a partially completed MOSFET in island 322, which would be just one of thousands of such devices in an integrated circuit fabricated on the bonded wafer." (Emphasis added) Clearly, the MOSFET depicted in FIG. 3g is located in and at the surface of device silicon layer 322, and, as one of many transistors included in an integrated circuit, would be connected with other transistors in the circuit.

In response to the assertion that the original specification never discloses doped buried layers, as claimed in claim 4, the Examiner's attention is respectfully directed to FIG. 6, which clearly depicts a buried layer in device silicon layer 602 abutting diamond first dielectric layer 613. The depicted first dielectric layer 613 comprising diamond also provides support for claim 5.

In response to the statement that the specification never discloses the homogeneous silicide layer, the device layer bonded to the silicide layer, the interconnected transistors, and the silicide comprising bonding material, as claimed in claim 10, the term "homogeneous" is deleted in the amending of claims 10-11, 13-15, and 17-18. The issue of interconnected transistors has already been dealt with in the discussion of claims 1 and 7 above. The remaining issues are resolved in the amendment of claim 10, which also responds to the assertion that the parent application never discloses the subject matter as claimed in claims 11-18. (As already noted, claim 12 is now canceled.)

New added claim 19 is supported in the specification at page 7, line 21 to page 8, line 11, and by FIGS. 4a-b and 5a-b. New added claims 20-21 are supported in the specification at page 9, lines 15-21, and page 10, lines 1-18. New claim 22 is supported at page 10, lines 28-31, and by FIGS. 4b-d and 5b.

In all previous Office Actions relating to the parent application, all claims have been rejected under 35 U.S.C. §103(a) as being unpatentable over the disclosure of Moslehi, U.S. Patent No. 5,102,821, ("Moslehi") in combination with the teachings of various other references. Similarly, in the August 3 Office Action, the disclosure of Moslehi has been combined with those of other references in the rejection of claims 1-6 and 10-17. There has been a persistent effort in the Office Actions to show substantial similarity between the bonded structure of the present invention, one embodiment of

which is depicted in Figures 4a-d, and the SOI wafer of Moslehi, represented in Figures 2a-f of the reference. Comparison of these figures and the supporting disclosures, however, reveals the gross dissimilarities between the applicants' structure and that of Moslehi.

As depicted in Figure 4b of the instant application, silicide layer 415, which overlies handle oxide layer 413, is a continuous, unpatterned layer of $CoSi_2$. Figure 4c illustrates trenches extending through the silicide layer to form islands each with an underlying continuous silicide area. The Moslehi structure, on the other hand, includes, as shown in Figures 2e-f , a layer containing both a semiconductor (silicide 40) and a metal (e.g. titanium 24) in a grid pattern over oxide layer 22.

Also, in the present invention, the silicide layer 415 lies between and is thereby adjacent to both first and second dielectric (oxide) layers 406 and 413, respectively, as shown in Figures 4b-d.. The thin (500 angstroms thick, cf. page 7, lines 25-31) unpatterned polysilicon layers 417 and 414 shown in Figure 4(a) are substantially consumed in the reaction with Co to form layer 415. In the Moslehi structure, by contrast, the grid-patterned layer containing silicide (40) and metal (24) is adjacent to only one oxide layer, 22 and overlies a corresponding grid pattern of relatively thick (2 μm, cf. column 3, lines 22-23), polysilicon 38 and micro-vacuum chambers 42.

The silicide layer 415 of the present invention constitutes a diffusion barrier to impurities. The metal-silicide grid structure of Moslehi, on the other hand, apparently does not function as a diffusion barrier, although the desirability of a such a feature is clearly recognized in the reference, as evidenced by the disclosure of and claims to a separate diffusion resistant layer of nitride adjacent to an oxide layer (cf. column 2, lines 28-30, claims 3-4).

The foregoing discussion makes clear the large and diverse discrepancies between the teachings of Moslehi and the present invention.

Claims 1-4, 10, 11, 13, 14, and 16 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Moslehi in view of See et al., U.S. Patent No. 5,212,397 ("See"). This rejection is respectfully traversed. The disclosure of See, which is relied on for its teaching of bipolar and MOS transistors formed on a silicon substrate, cannot remedy the gross deficiencies in the teachings of Moslehi. Withdrawal of the §103(a)

rejection of claims 1-4, 10, 11,13, 14, and 16 as unpatentable over this combination of references is respectfully requested.

Claims 5, 6, and 15-17 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Moslehi in view of See, and further in view of Sugimoto et al., JP 2-206118 ("Sugimoto"). Claim 6 is canceled; the rejection of claims 5 and 15-17 is respectfully traversed. The addition of Sugimoto solely for its disclosure of diamond dielectric layer does not compensate for the already noted deficiencies of the other two references. Withdrawal of the rejection of claims 5 and 15-17 is respectfully requested.

The §103(a) rejection of claim 12 as unpatentable over Moslehi, See, and Iwamatsu is moot in light of the cancellation of this claim.

Claims 7-10 and 16-18 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Ochiai, U.S. Patent No. 5,378,919 ("Ochiai") in view of Kameyama et al., JP 1-73659 ("Kameyama"). This rejection is respectfully traversed.

Ochiai discloses an integrated circuit device with an SOI structure and comprising a plurality of transistors, each overlying a resistance layer [52]. The Ochiai semiconductor structure is a "sea-of-gate array" and thus includes no trenches to define device islands. Also, as acknowledged in the Office Action, the reference does not show that the resistance layer comprises a silicide. In fact, Ochiai makes no mention whatsoever of silicides. Although not explicitly stated, the resistance layer [52] of Ochiai appears to be formed from polysilicon. Some embodiments of the present invention make use of transient thin polysilicon layers in their fabrication, but these are substantially completely consumed in the formation of the silicide layer that bonds the handle die to the device wafer.

The deficiency in the teaching of Ochiai is not remedied by the disclosure in Kameyama of a polycrystalline tungsten silicide resistor thin film, which is formed between two oxide layers and has aluminum electrodes connected at both ends. Withdrawal of the §103(a) rejection of claims 7-10 and 16-18 as unpatentable over Ochiai and Kameyama is therefore respectfully requested.

Claims 1-5, 7-11, and 13-22 are now in this case. In light of the foregoing Amendment and Remarks, prompt allowance of this application is earnestly solicited.

Respectfully submitted,

11/2/99
Date

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